

IRF7811A

HEXFET® Power MOSFET

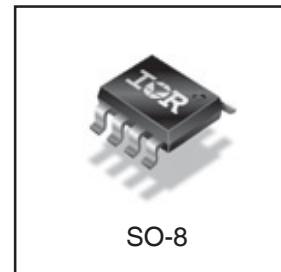
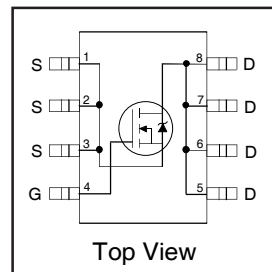
Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- 100% R_G Tested

V _{DSS}	R _{DS(on)} max	Q _g
28V	12mΩ	17nC

Benefits

- Very Low R_{DS(on)} at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max	Units
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	11 ^④	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	9.1 ^④	
I _{DM}	Pulsed Drain Current ^①	91	
P _D @ T _A = 25°C	Power Dissipation ^④	2.5	W
P _D @ T _A = 70°C	Power Dissipation ^④	1.6	
	Linear Derating Factor	0.02	W/°C
V _{GS}	Gate-to-Source Voltage	±12	V
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Smoldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
R _{θJL}	Junction-to-Drain Lead ^⑤	—	20	°C/W
R _{θJA}	Junction-to-Ambient ^{④⑤}	—	50	

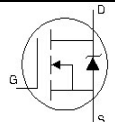
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	28	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.025	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	8.7	10	mΩ	V _{GS} = 10V, I _D = 11A ④
		—	10	12		V _{GS} = 4.5V, I _D = 9.0A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-4.0	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	12	μA	V _{DS} = 28V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 100°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -12V
g _{fs}	Forward Transconductance	28	—	—	S	V _{DS} = 15V, I _D = 9.0A
Q _g	Total Gate Charge	—	17	26	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 9.0A See Fig. 16
Q _{gs1}	Pre-V _{th} Gate-Source Charge	—	3.3	—		
Q _{gs2}	Post-V _{th} Gate-Source Charge	—	1.3	—		
Q _{gd}	Gate-to-Drain Charge	—	4.7	—		
Q _{godr}	Gate Charge Overdrive	—	7.2	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	6.0	—		
Q _{oss}	Output Charge	—	24	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	0.9	—	3.7	Ω	
t _{d(on)}	Turn-On Delay Time	—	7.5	—	ns	V _{DD} = 15V, V _{GS} = 4.5V ④ I _D = 9.0A Clamped Inductive Load
t _r	Rise Time	—	4.1	—		
t _{d(off)}	Turn-Off Delay Time	—	19	—		
t _f	Fall Time	—	6.5	—		
C _{iss}	Input Capacitance	—	1760	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	960	—		
C _{riss}	Reverse Transfer Capacitance	—	54	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	58	mJ
I _{AR}	Avalanche Current ①	—	9.0	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	91		
V _{SD}	Diode Forward Voltage	—	0.8	1.0	V	T _J = 25°C, I _S = 9.0A, V _{GS} = 0V③
		—	0.66	—		T _J = 125°C, I _S = 9.0A, V _{GS} = 0V③
t _{rr}	Reverse Recovery Time	—	72	110	ns	T _J = 25°C, I _F = 9.0A, V _R = 15V
Q _{rr}	Reverse Recovery Charge	—	93	140	nC	di/dt = 100A/μs ③
t _{rr}	Reverse Recovery Time	—	73	110	ns	T _J = 125°C, I _F = 9.0A, V _R = 15V
Q _{rr}	Reverse Recovery Charge	—	100	150	nC	di/dt = 100A/μs ③

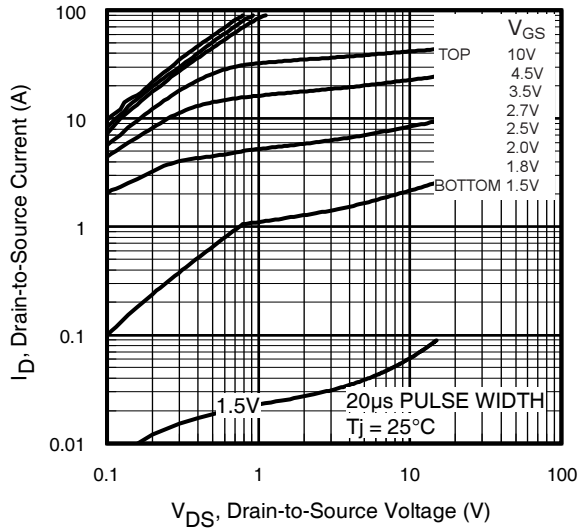


Fig 1. Typical Output Characteristics

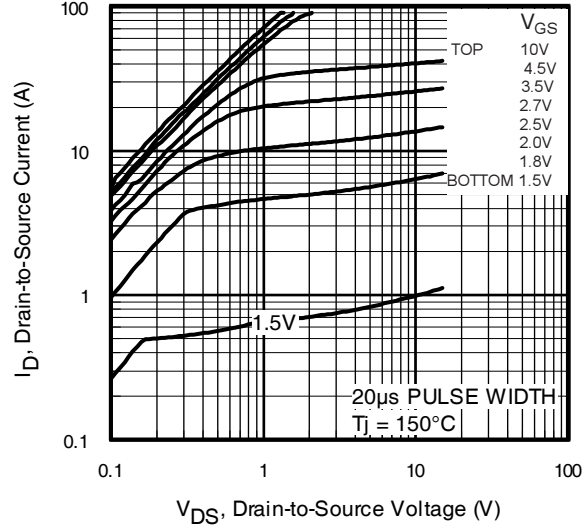


Fig 2. Typical Output Characteristics

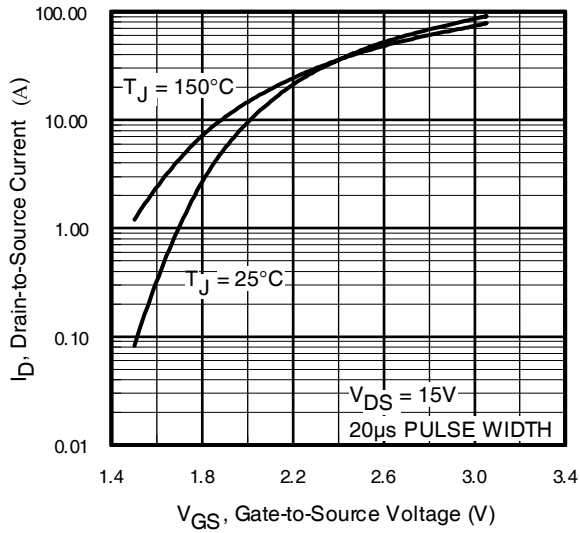


Fig 3. Typical Transfer Characteristics

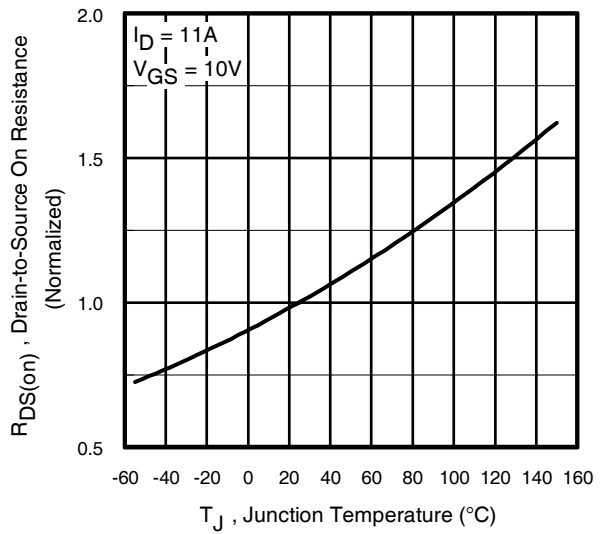


Fig 4. Normalized On-Resistance Vs. Temperature

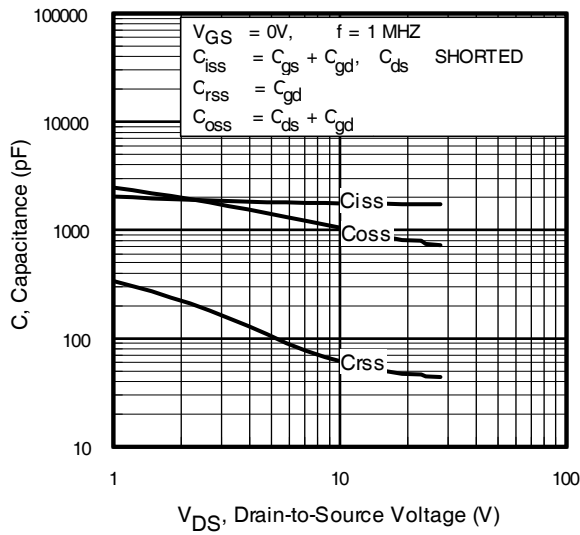


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

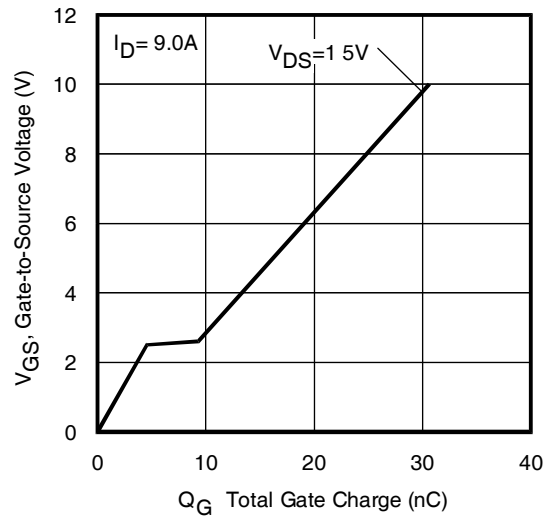


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

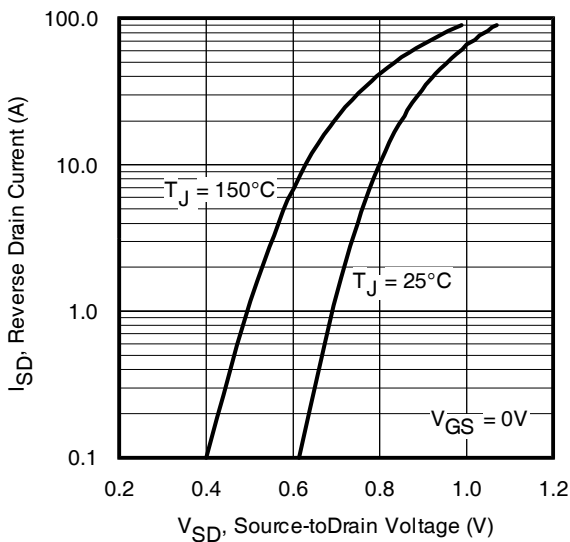


Fig 7. Typical Source-Drain Diode Forward Voltage

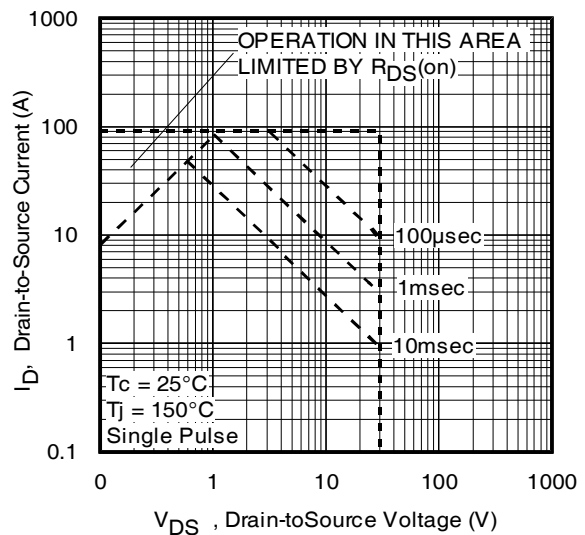


Fig 8. Maximum Safe Operating Area

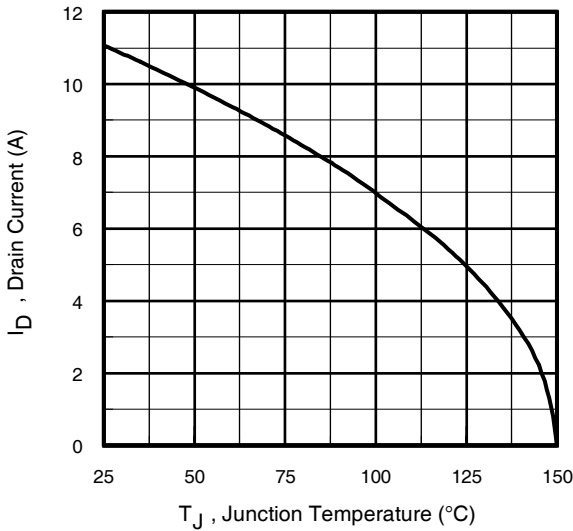


Fig 9. Maximum Drain Current Vs. Ambient Temperature

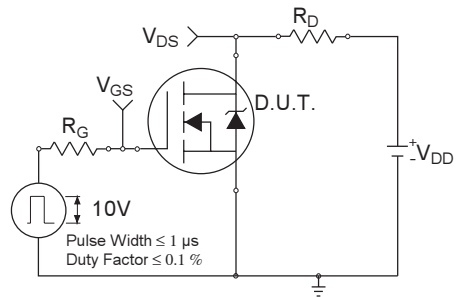


Fig 10a. Switching Time Test Circuit

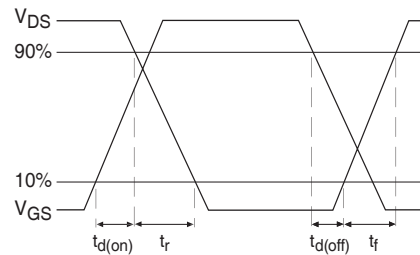


Fig 10b. Switching Time Waveforms

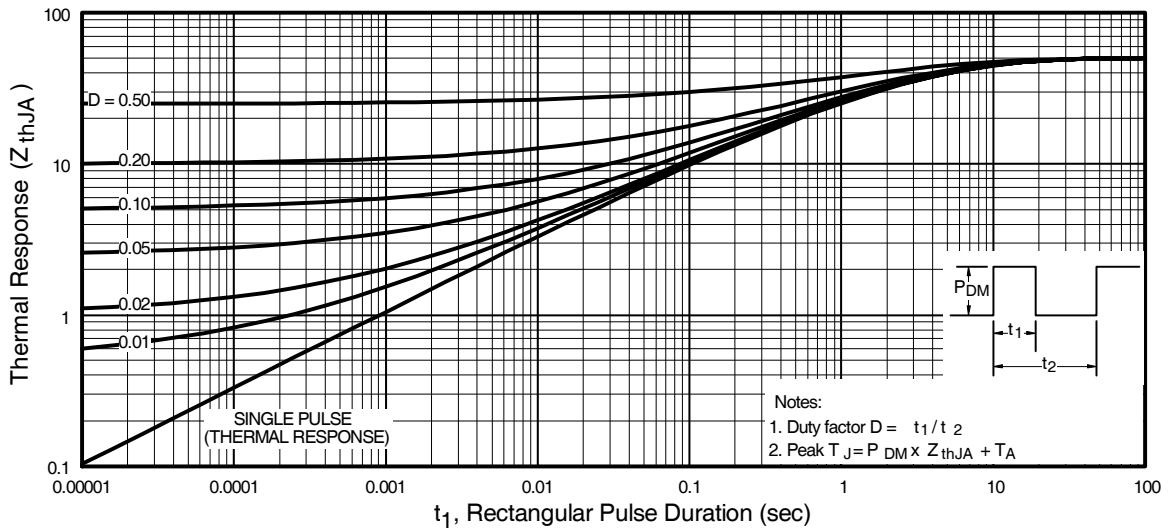


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

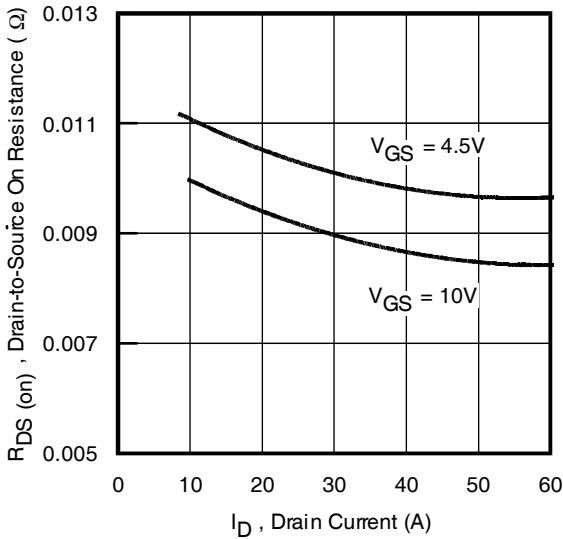


Fig 12. On-Resistance Vs. Drain Current

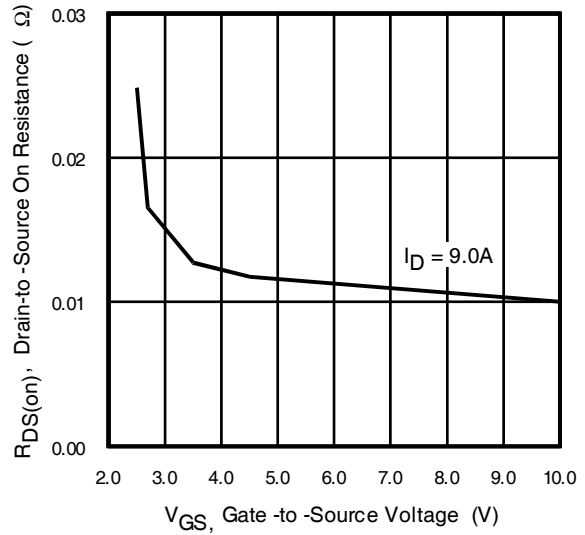


Fig 13. On-Resistance Vs. Gate Voltage

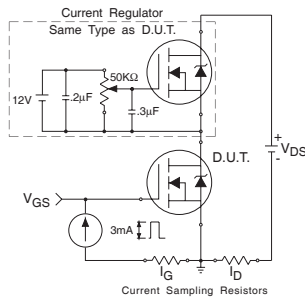


Fig 14. Basic Gate Charge Test Circuit

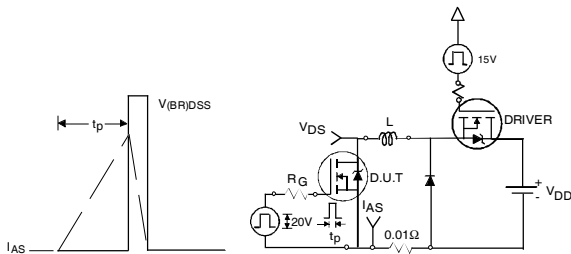


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

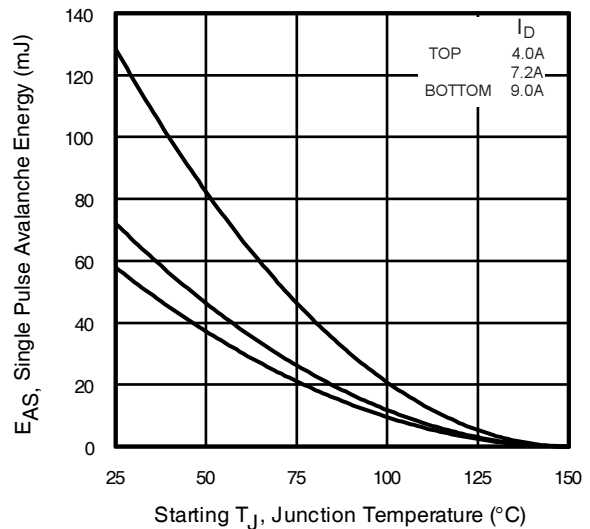


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

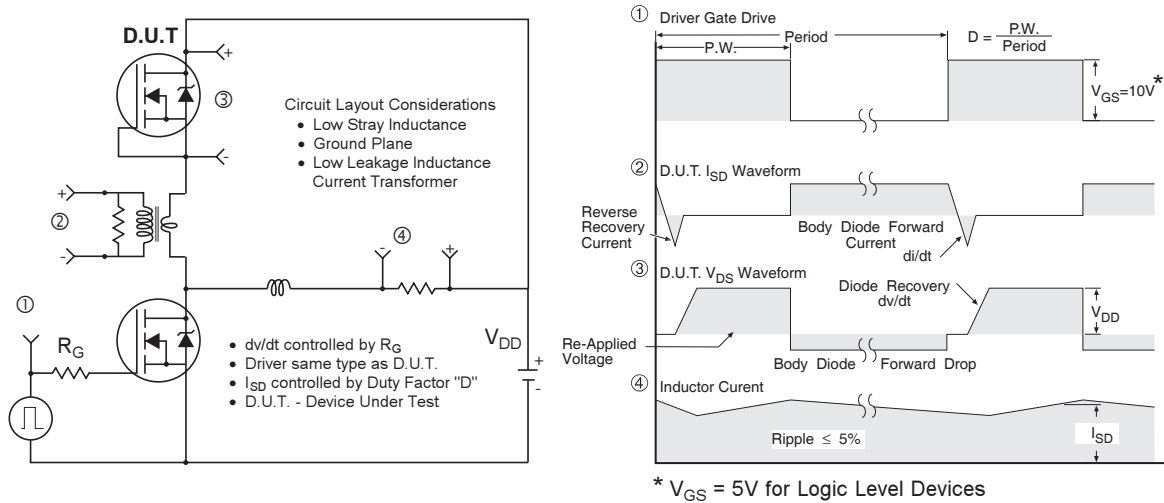


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

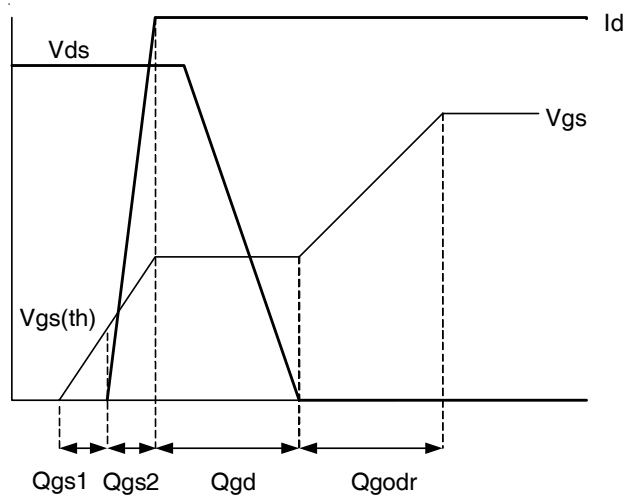


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + (Q_{rr} \times V_{in} \times f)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

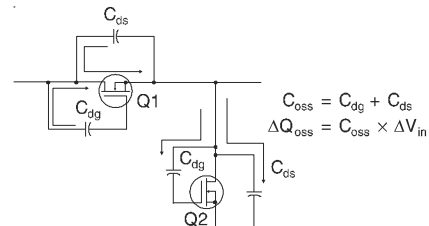
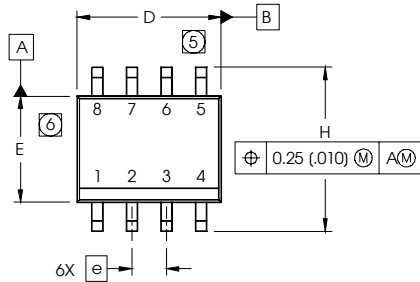


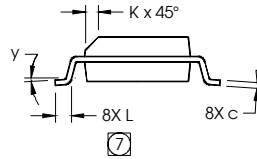
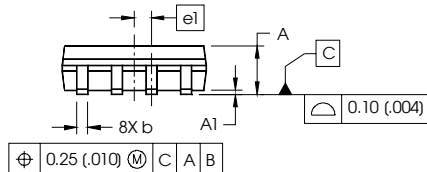
Figure A: Q_{oss} Characteristic

SO-8 Package Details

Dimensions are shown in millimeters (inches)



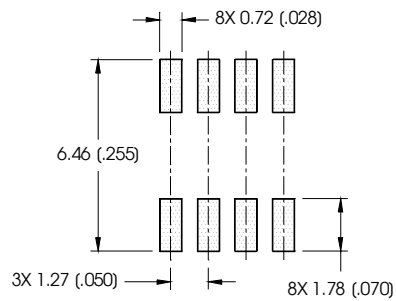
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

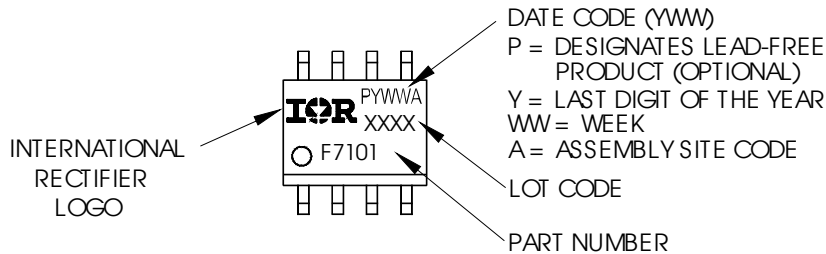
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

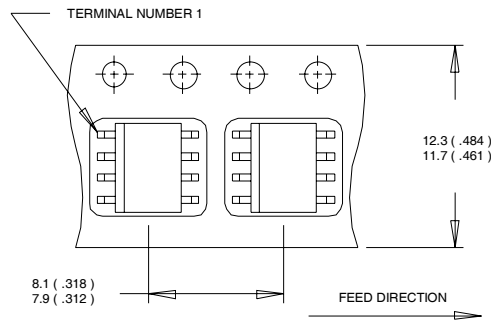
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



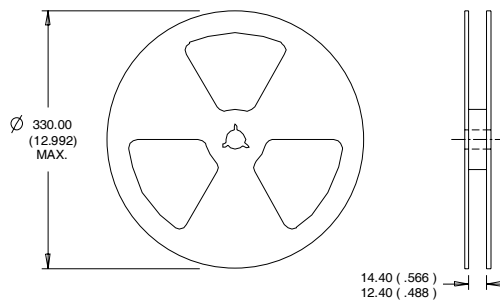
IRF7811A

International
IR Rectifier

SO-8 Tape and Reel



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.4\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 9.0\text{A}$.
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board
- ⑤ R_θ is measured at T_J approximately at 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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TAC Fax: (310) 252-7903

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